

This cross-sectional view shows a central gate structure 30 with a top layer 36, an intermediate layer 34, and a bottom layer 32. The gate is flanked by side spacers 28. The spacers are composed of a bottom layer 22, a middle layer 20, and a top layer 16. The spacers are separated by a gap 24. The entire structure is built on a substrate 10. The central gate structure is labeled 38, and the side spacers are labeled 26a and 26b. A dashed line C indicates a cross-section through the central gate structure.

This cross-sectional view shows a central gate structure 30 with a top layer 36, a middle layer 34, and a bottom layer 32. The gate is flanked by side spacers 40. The device is built on a substrate 10 with a base layer 12. A layer 24 is formed on the substrate, containing regions 14, 16, and 20. A layer 22 is on top of 24. A dashed circle D indicates a specific area. Labels 26a and 26b point to the base of the side spacers. Arrows 38 point to the top of the side spacers.

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FIG. 2A

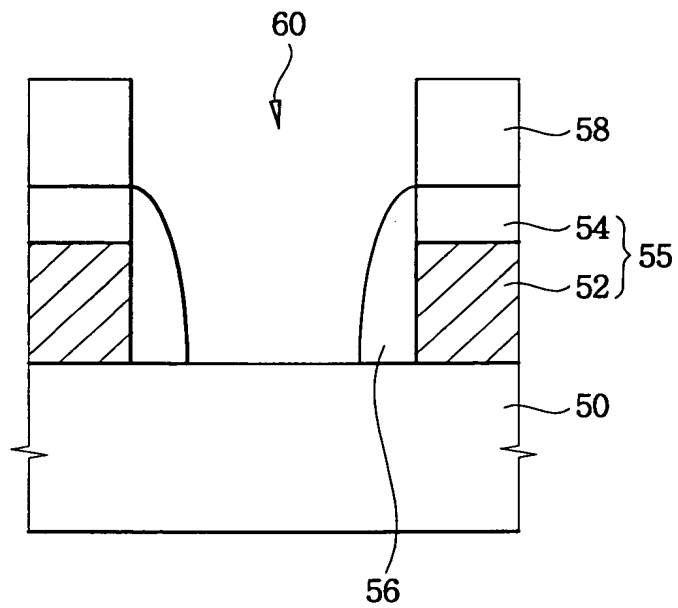
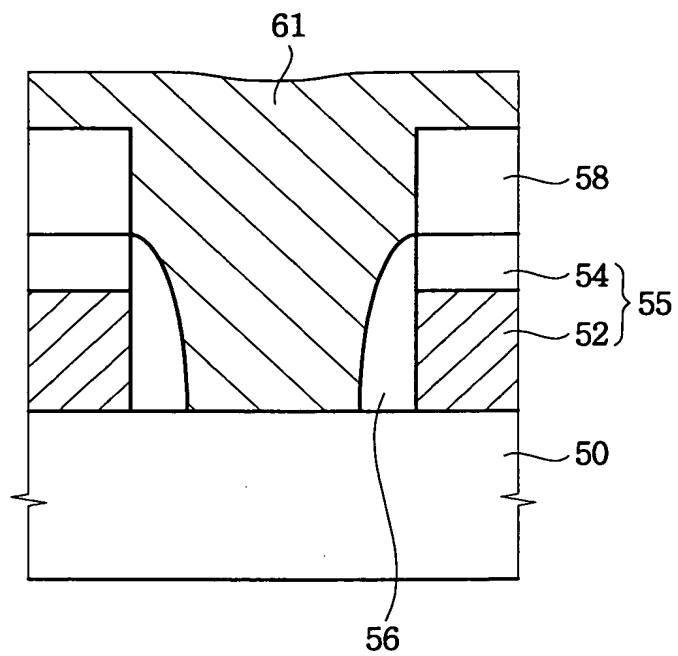


FIG. 2B



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FIG. 2C

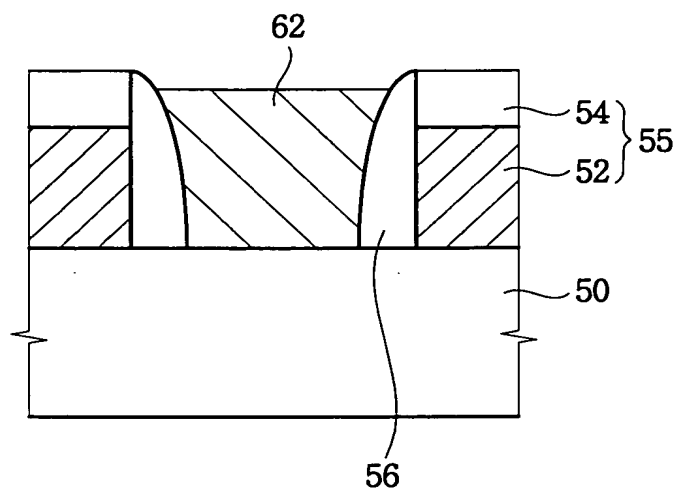
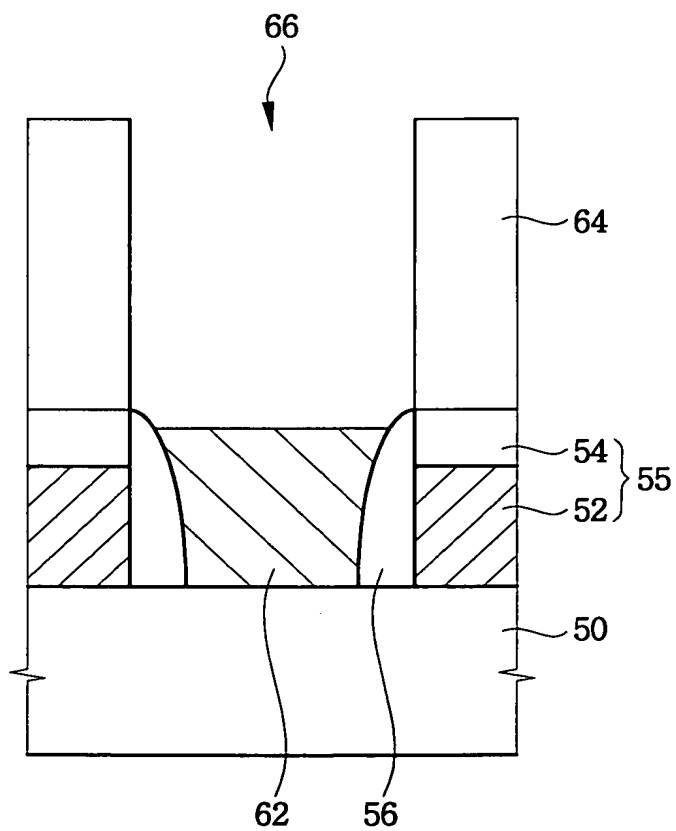
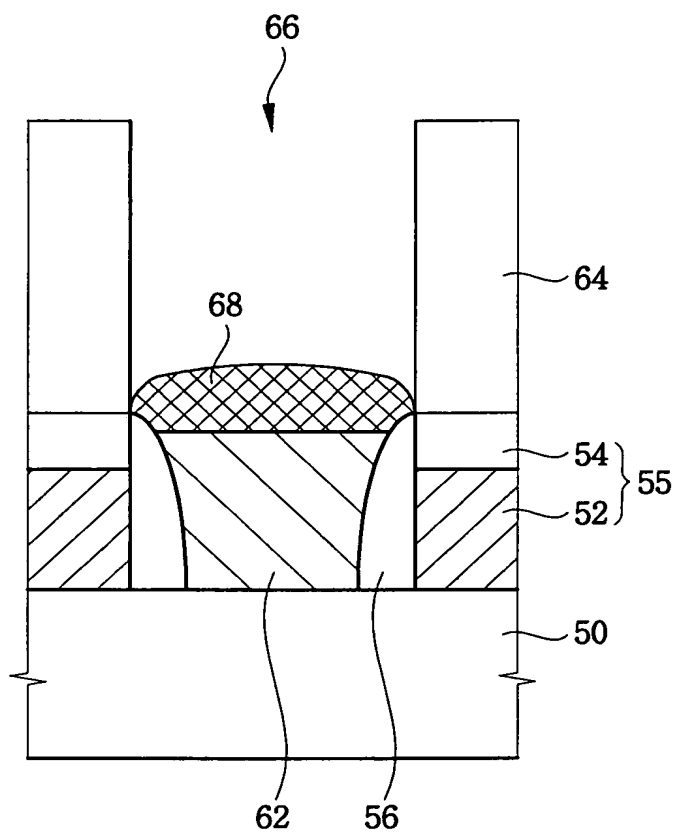


FIG. 2D



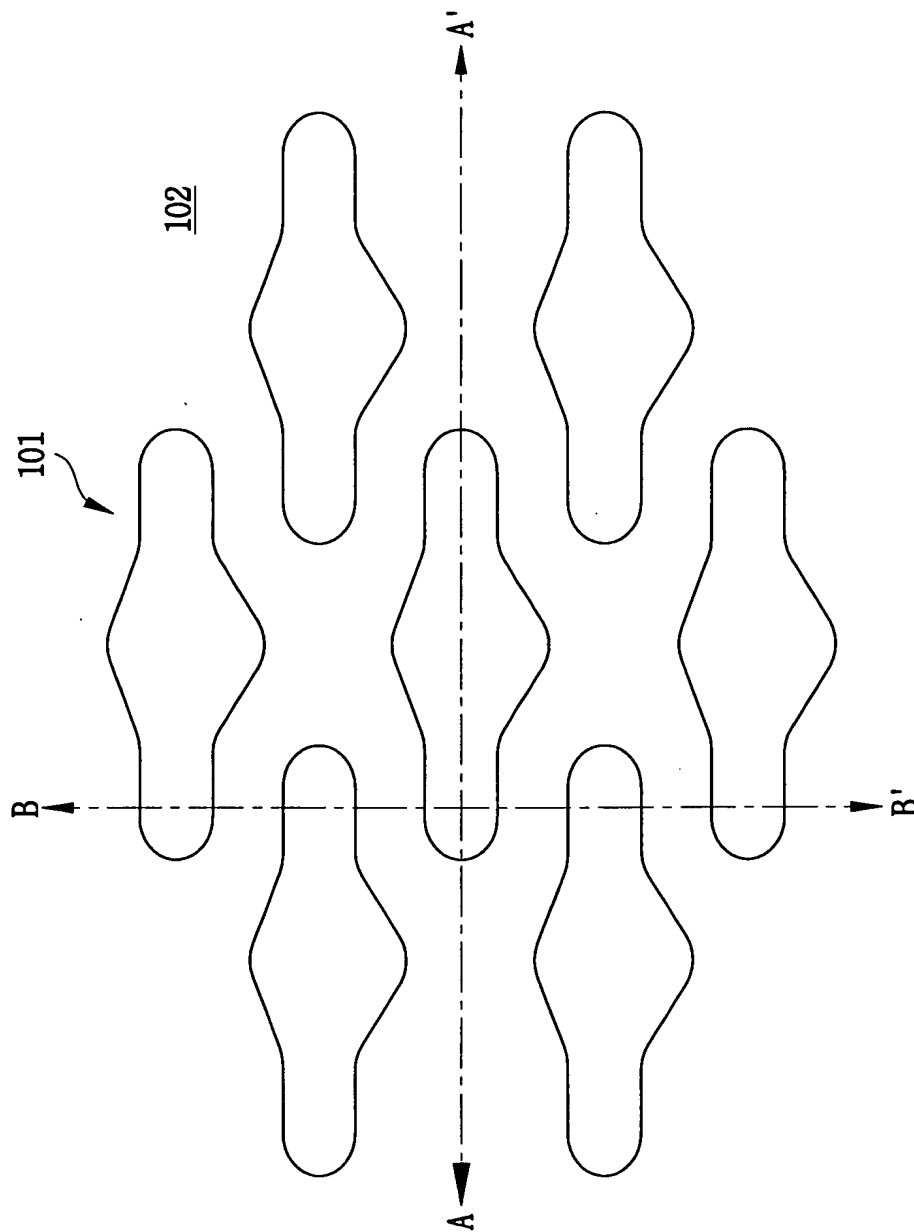
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FIG. 2E



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FIG. 3A



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FIG. 3B

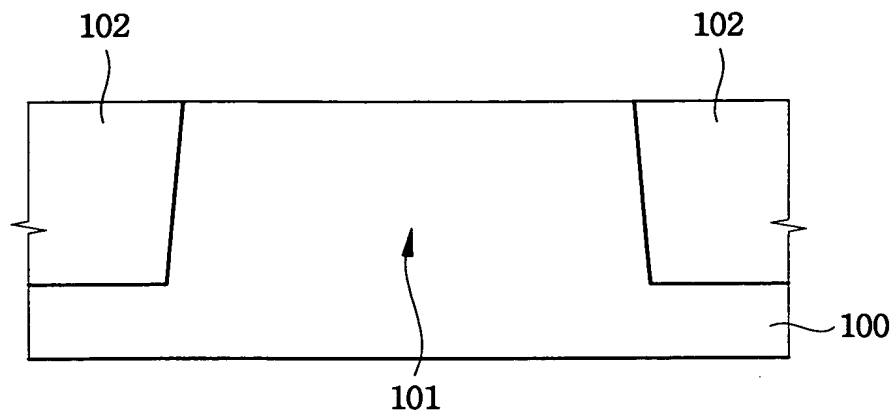


FIG. 3C

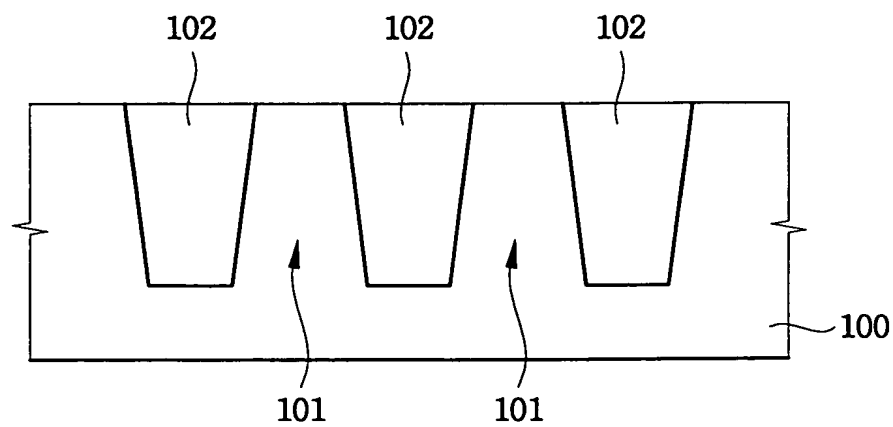
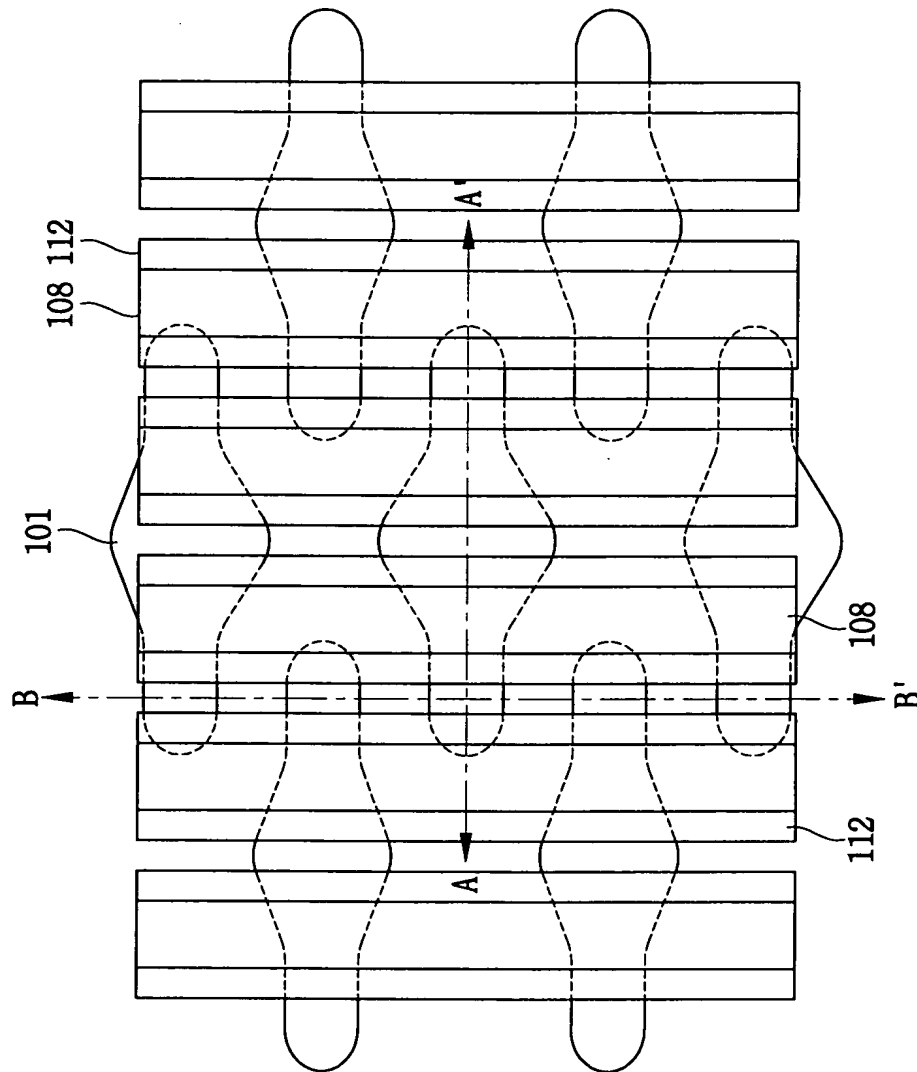


FIG. 4A





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FIG. 4B

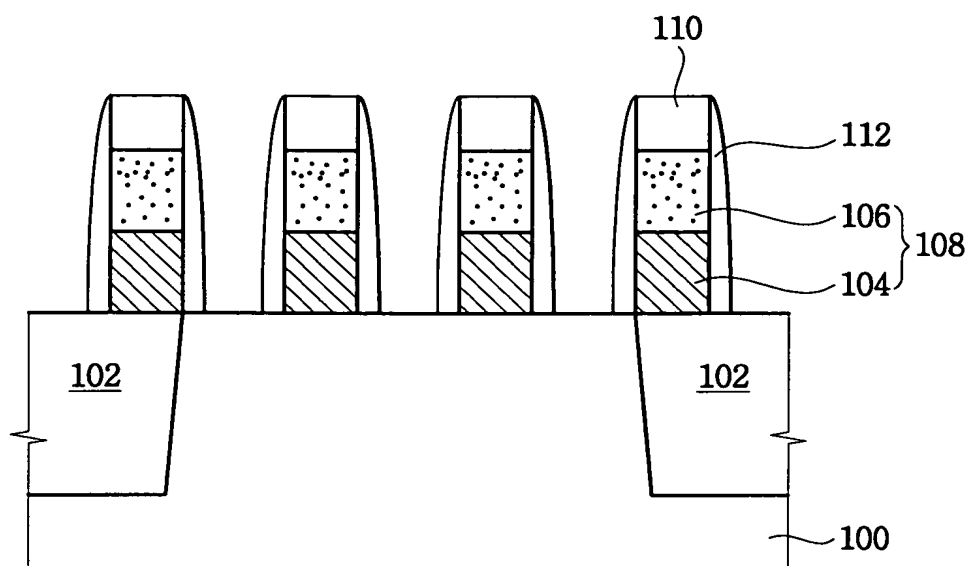
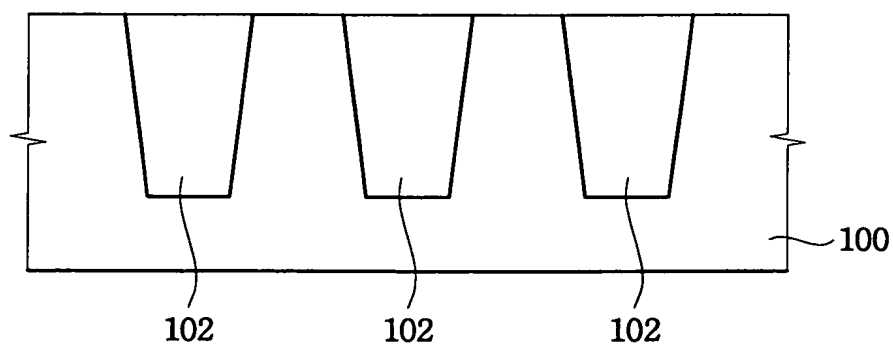
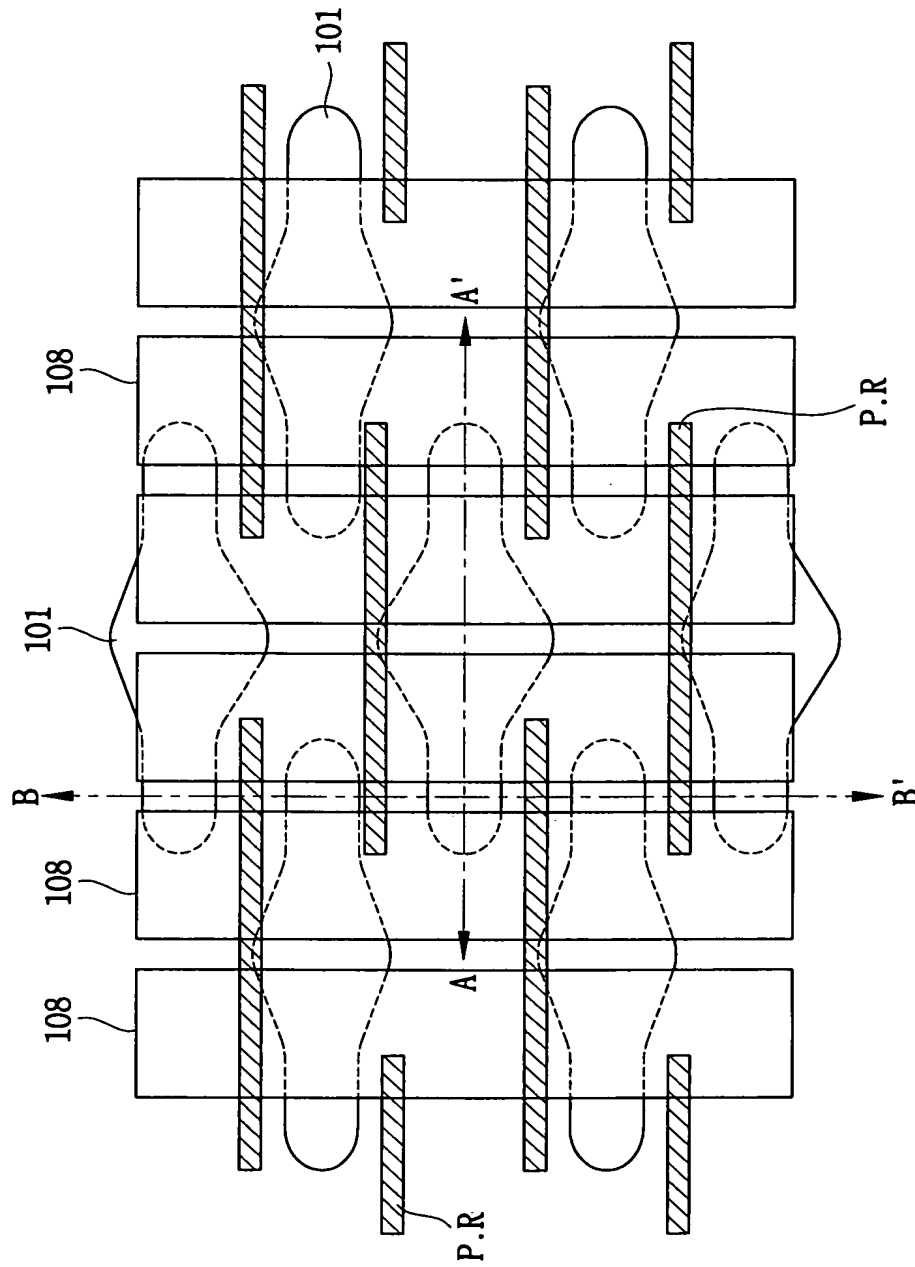


FIG. 4C



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FIG. 5A



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FIG. 5B

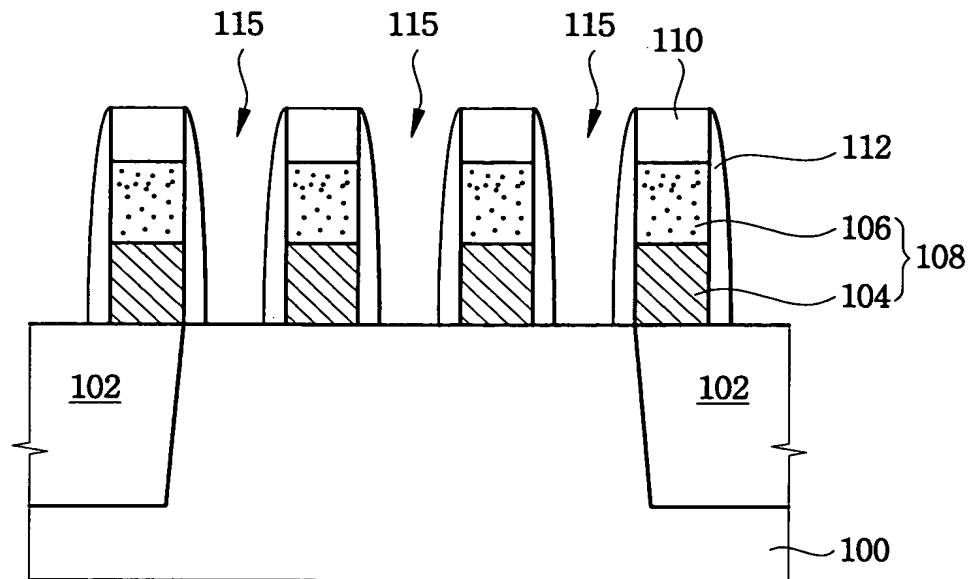
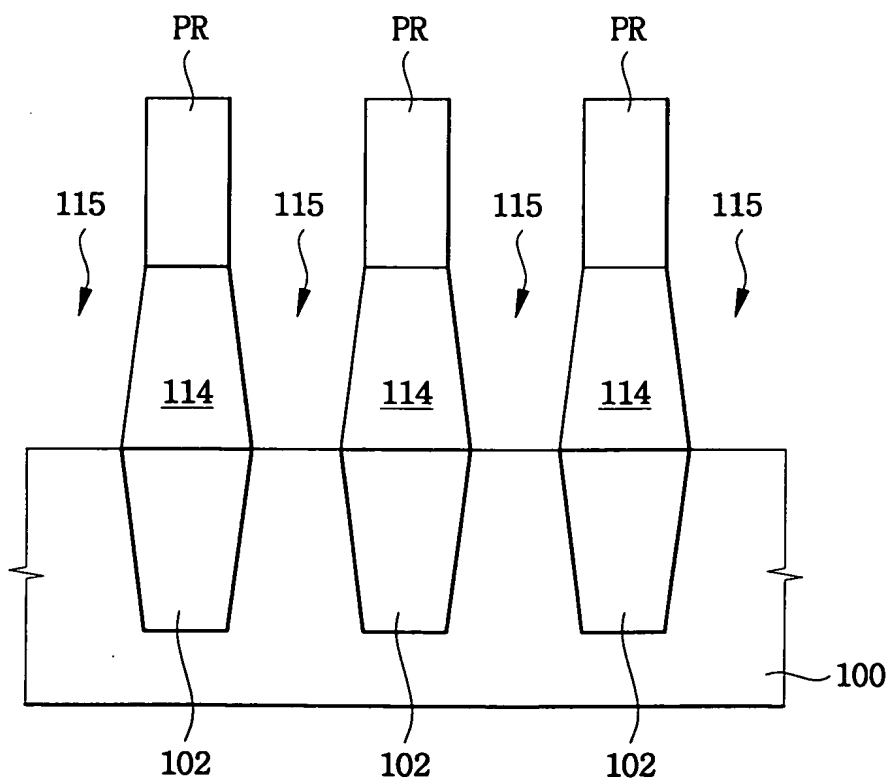
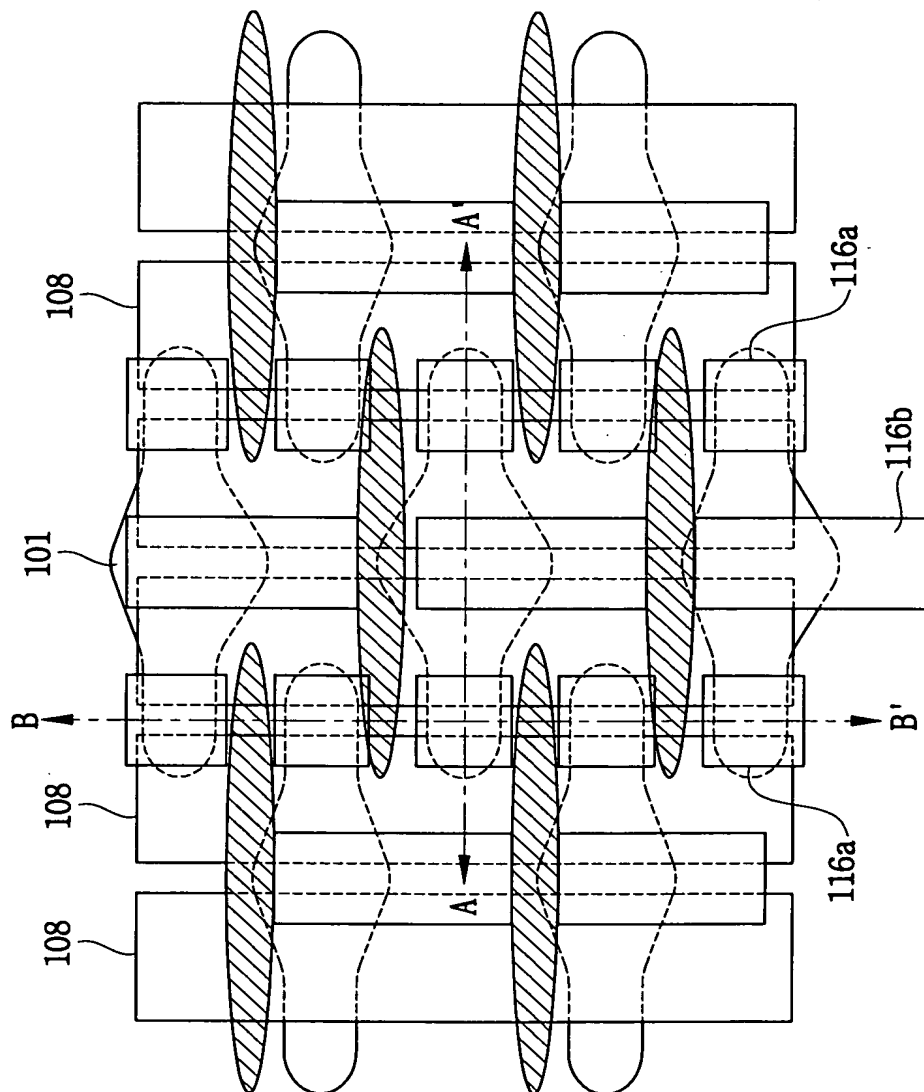


FIG. 5C



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FIG. 6A



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FIG. 6B

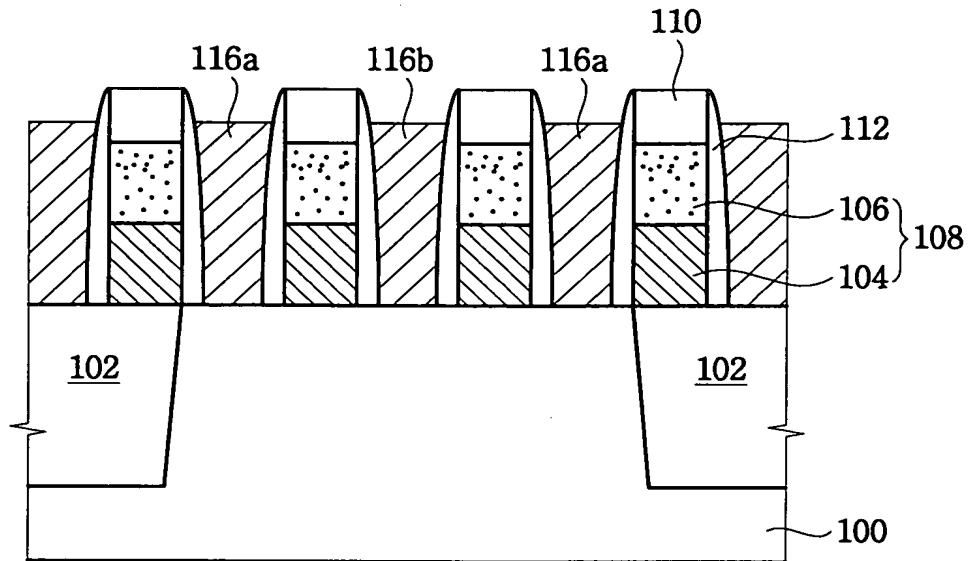


FIG. 6C

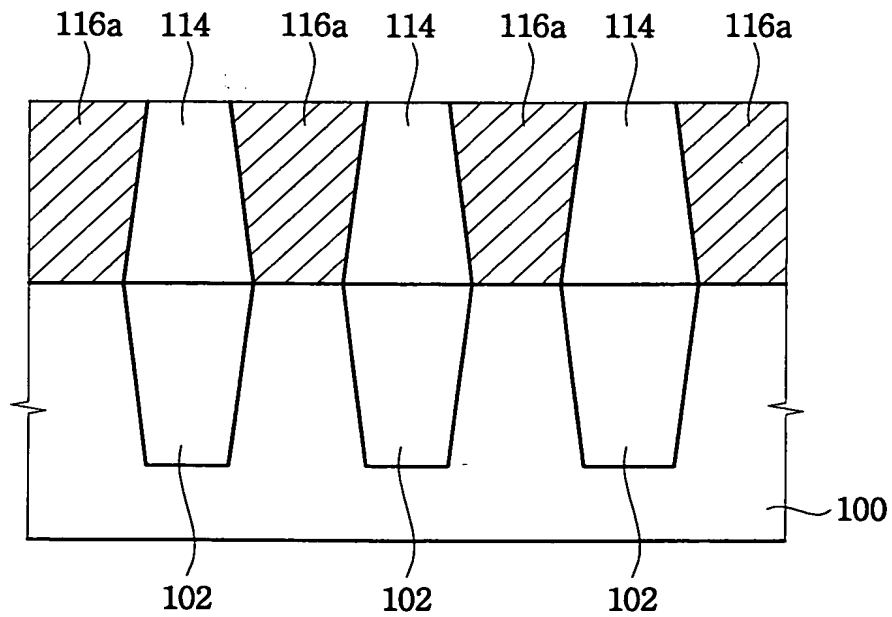
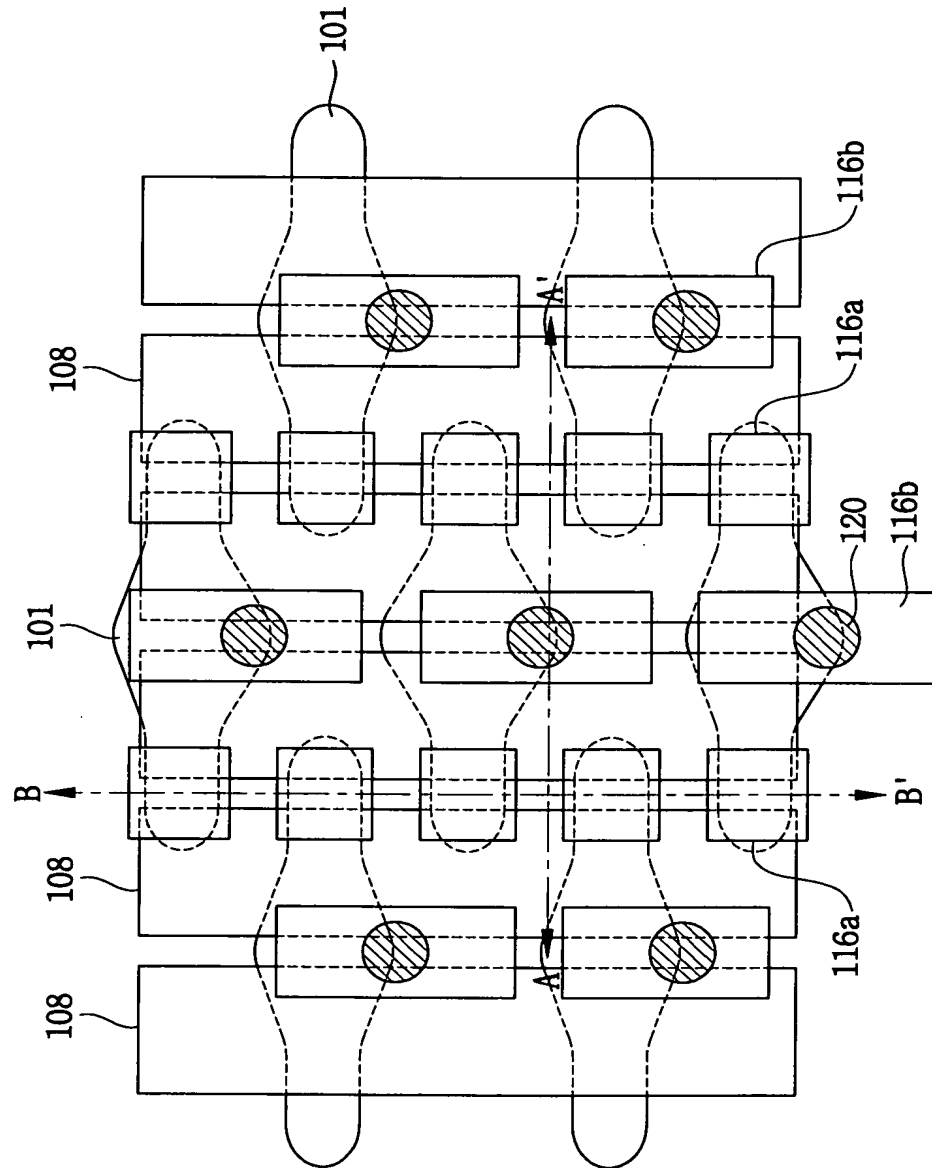
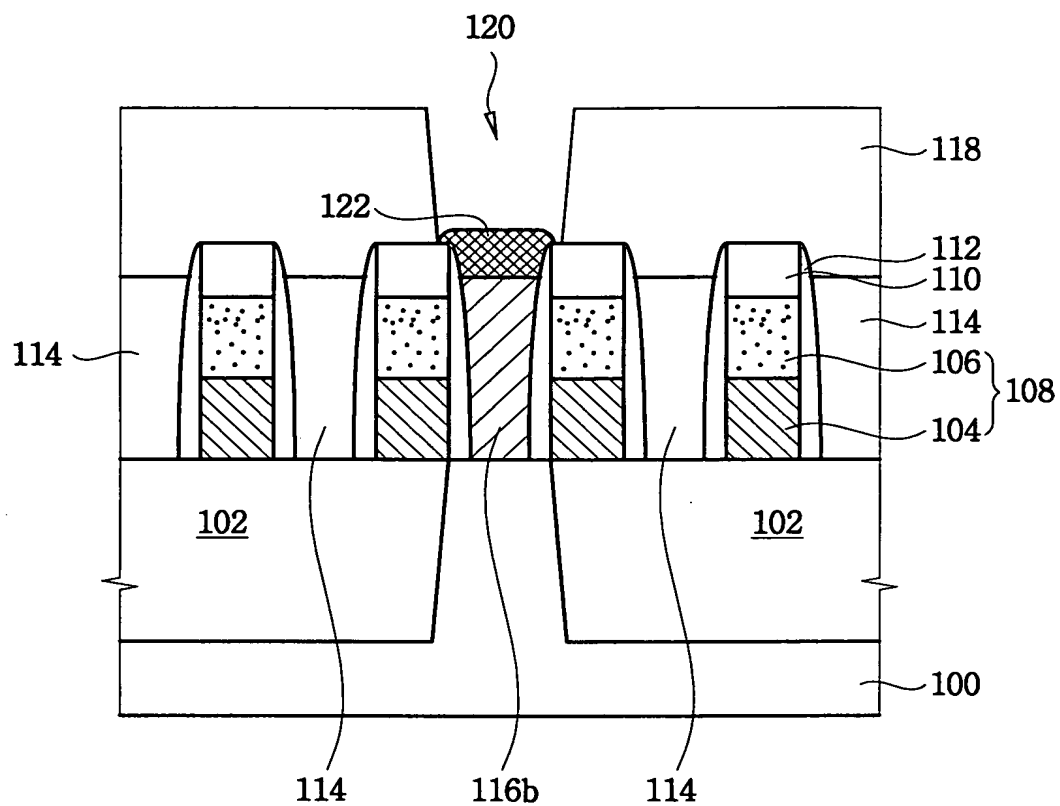


FIG. 7A



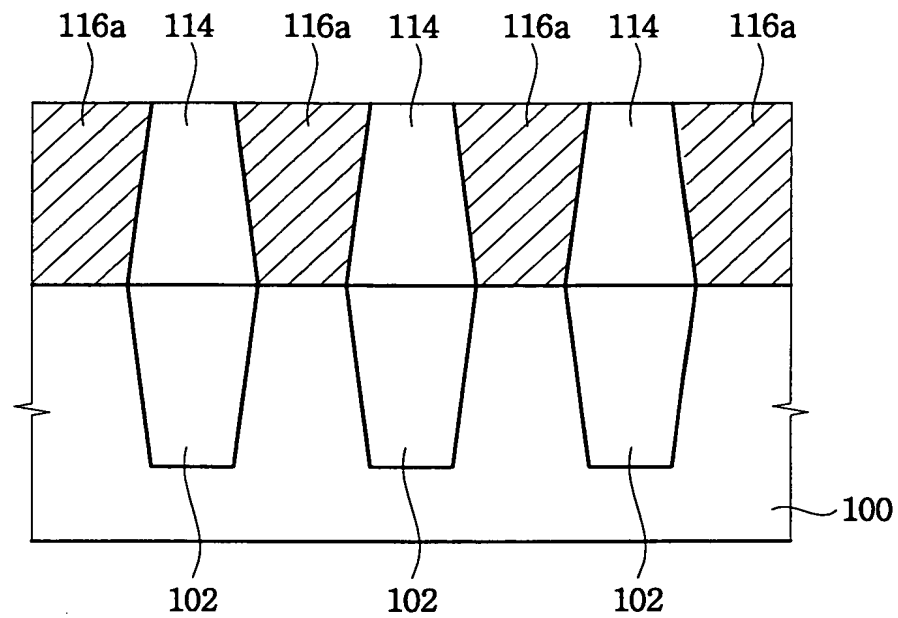
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FIG. 7B



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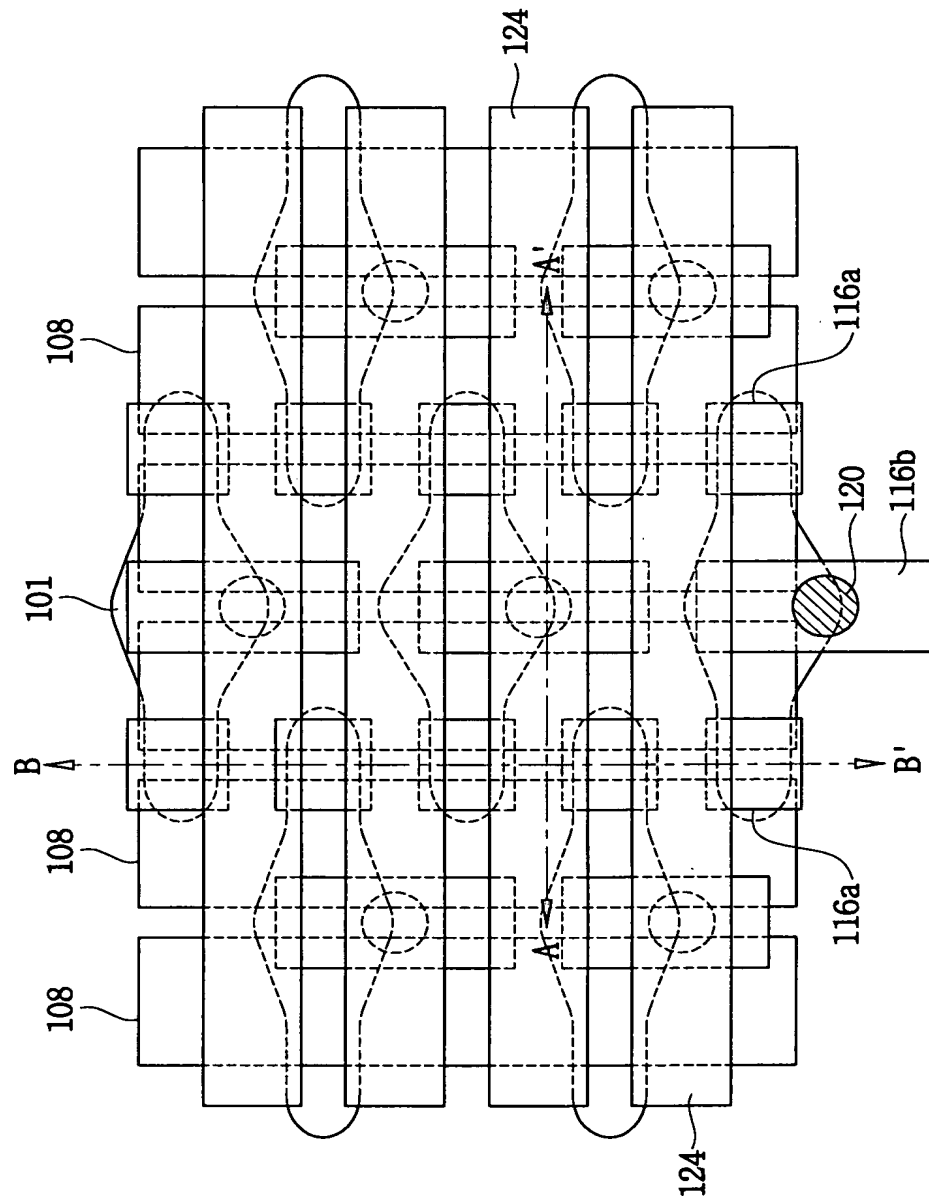
FIG. 7C





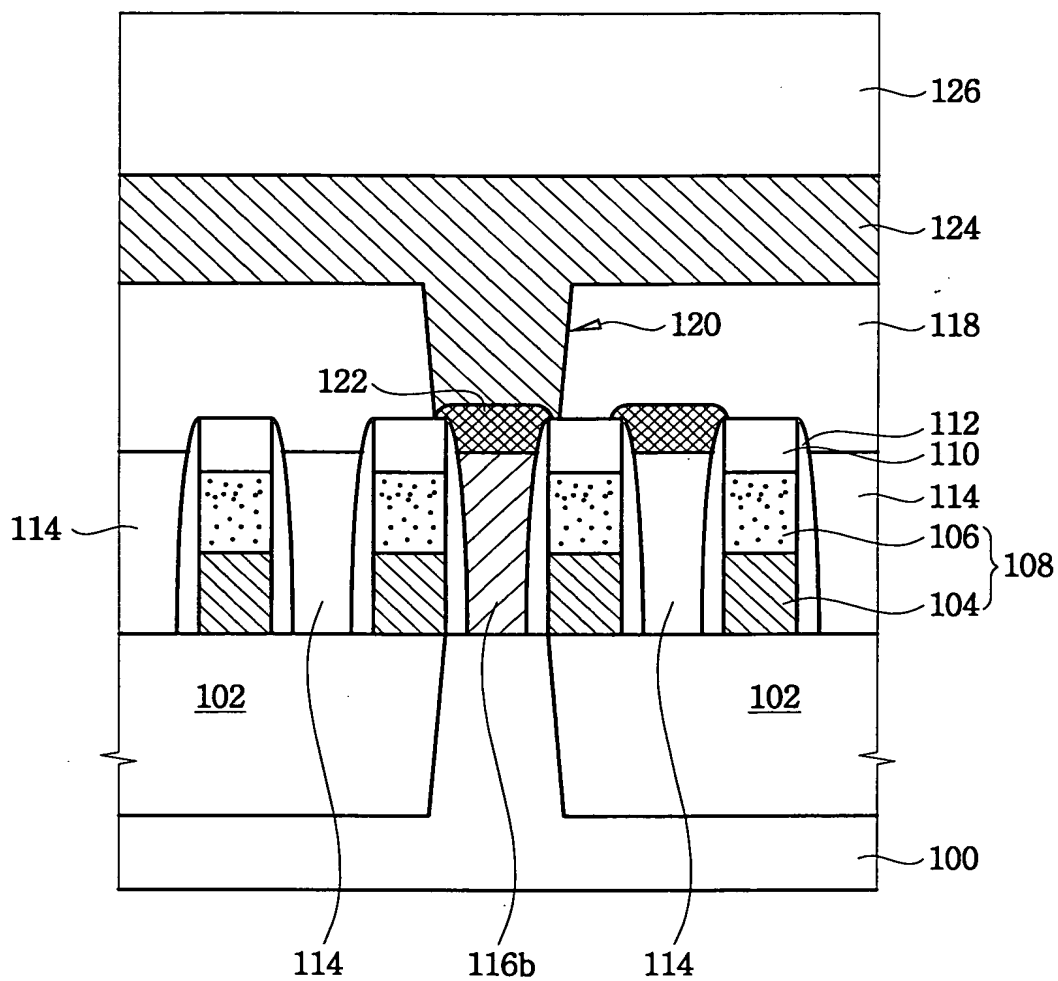
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FIG. 8A



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FIG. 8B



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FIG. 8C

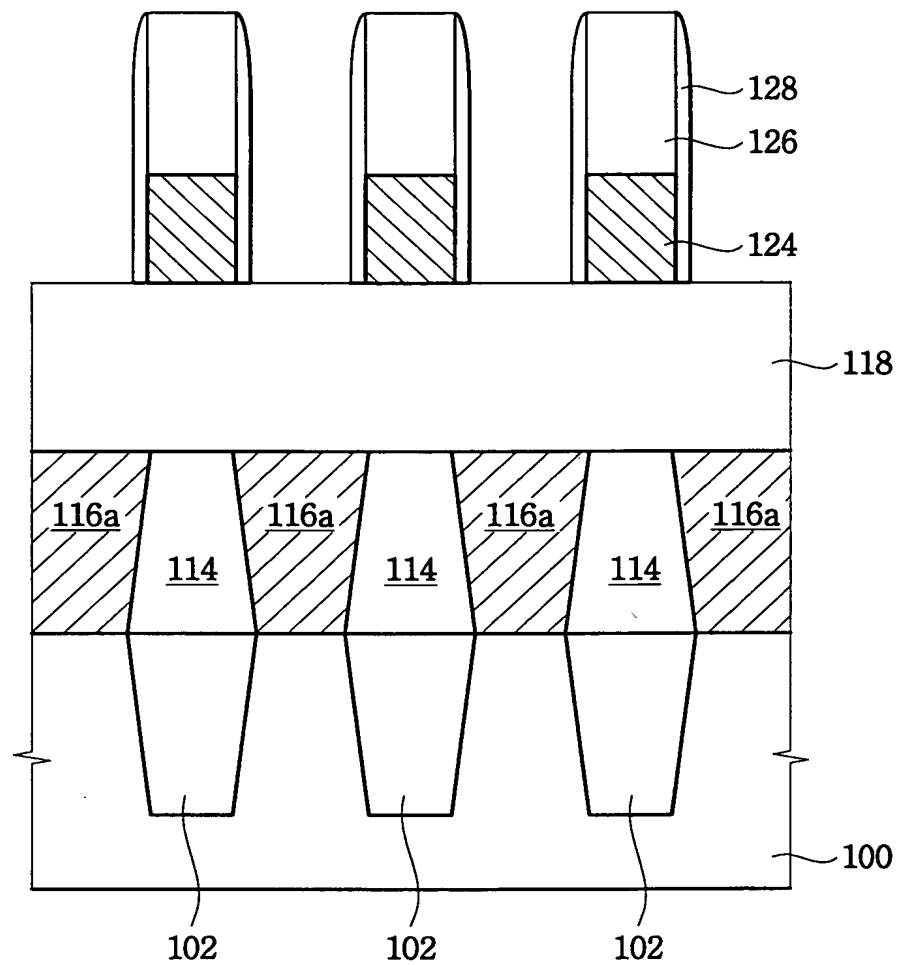
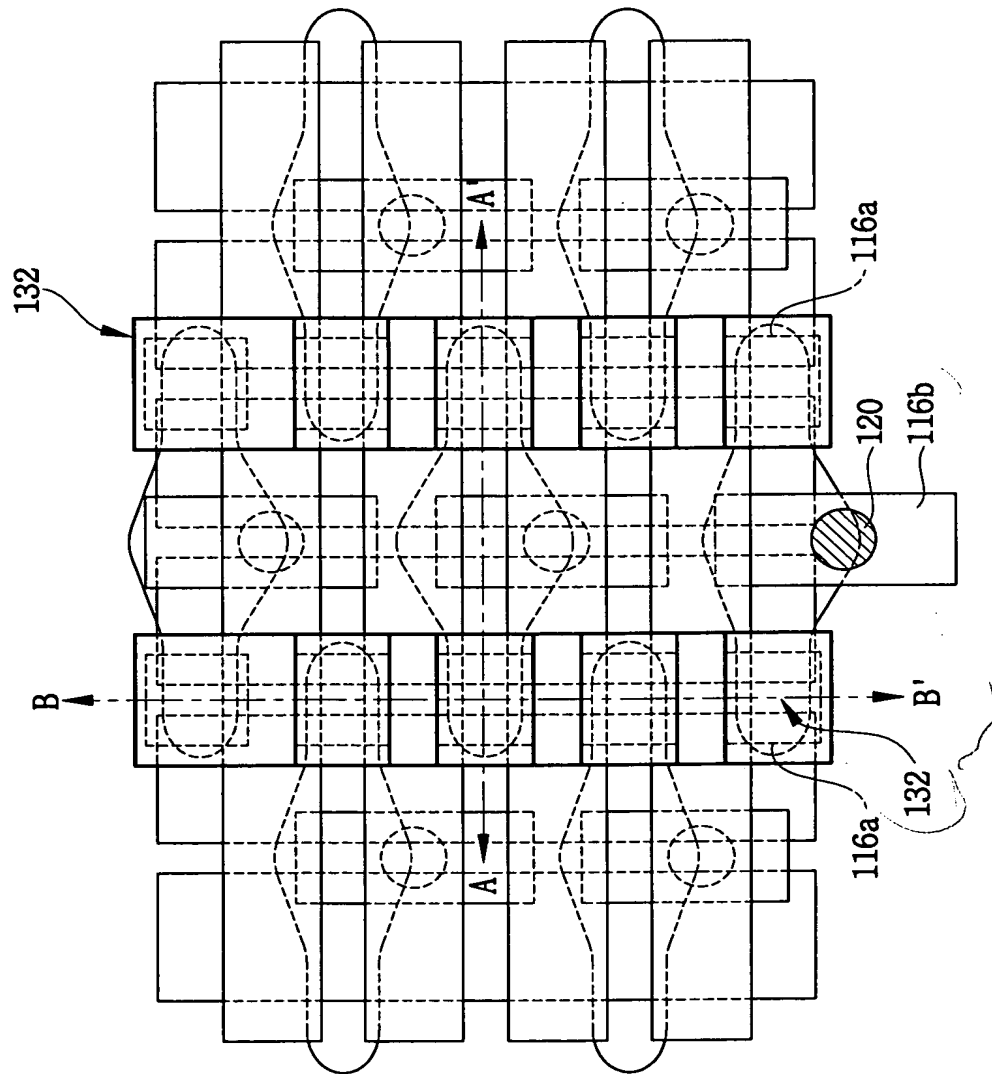
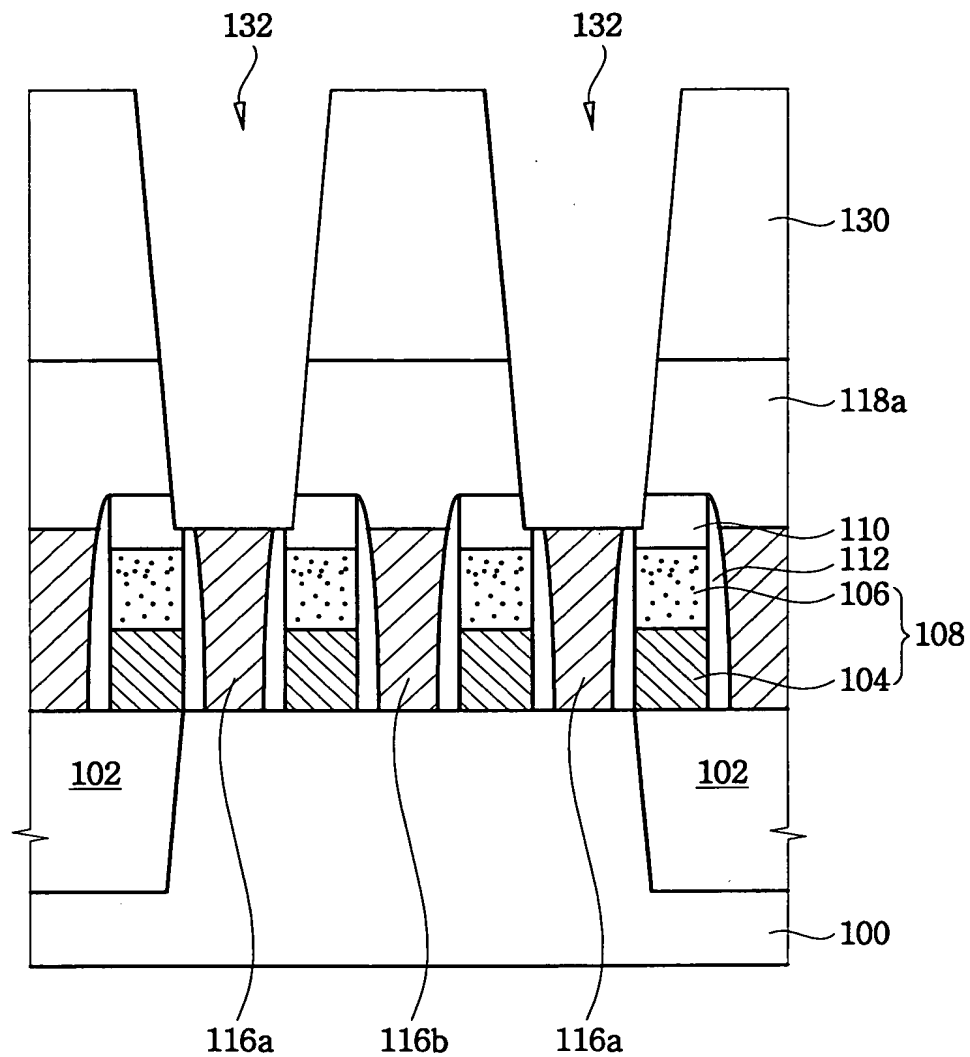


FIG. 9A



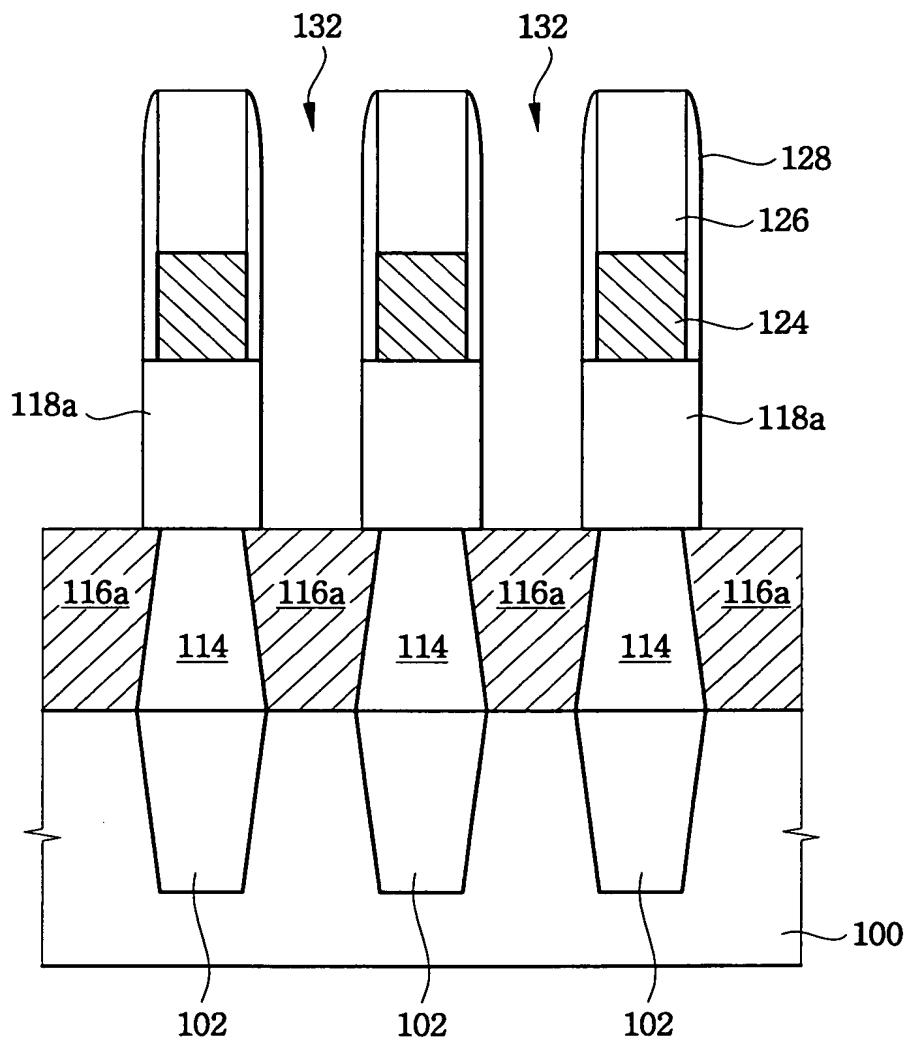
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FIG. 9B



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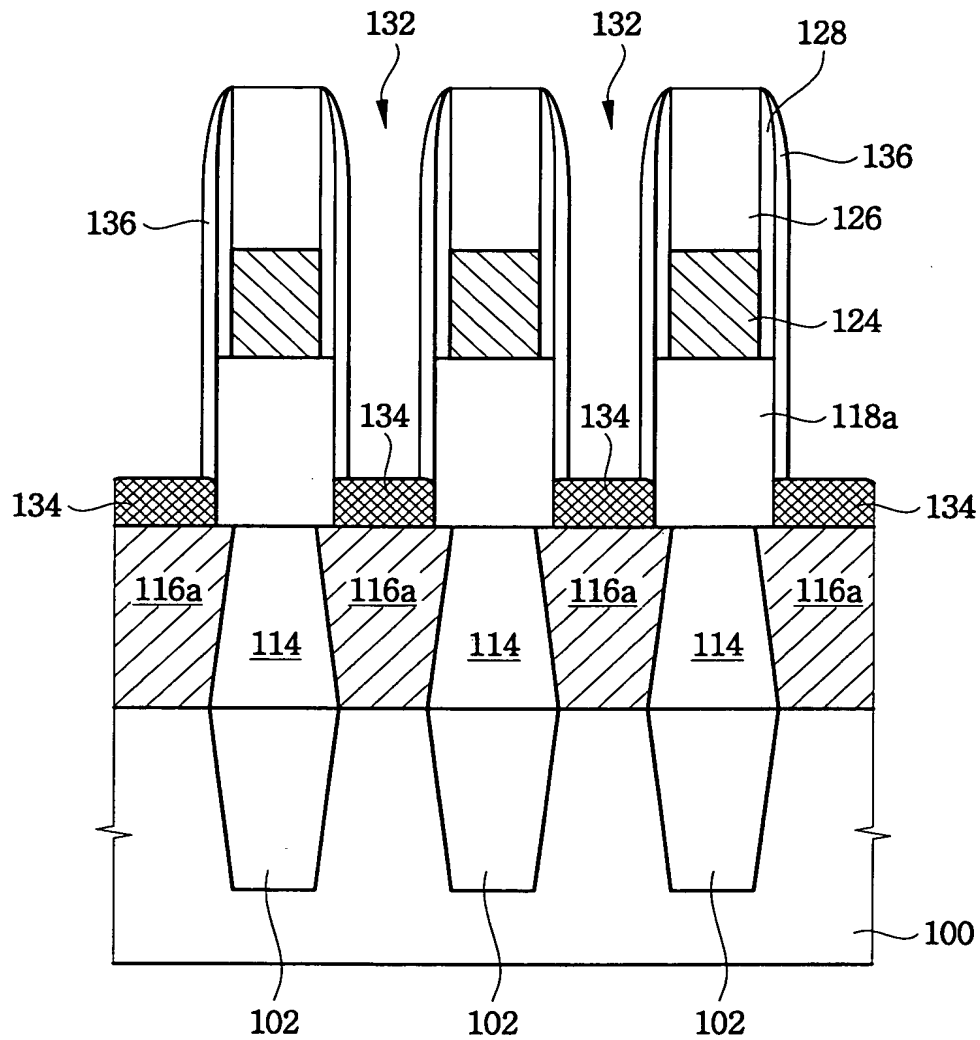
FIG. 9C



This cross-sectional view shows a substrate 100 with a trench array 102. The trench walls are labeled 104. A stack of layers 106, 110, 112, and 118a is formed on the trench bottom and walls. A conductive layer 130 is deposited on top. A patterned layer 132 is formed on the conductive layer 130, with its top surface labeled 136. The layer 132 is shown in cross-section as a series of rectangular blocks 134. The trench bottom is labeled 116a, and the trench walls are labeled 116b.

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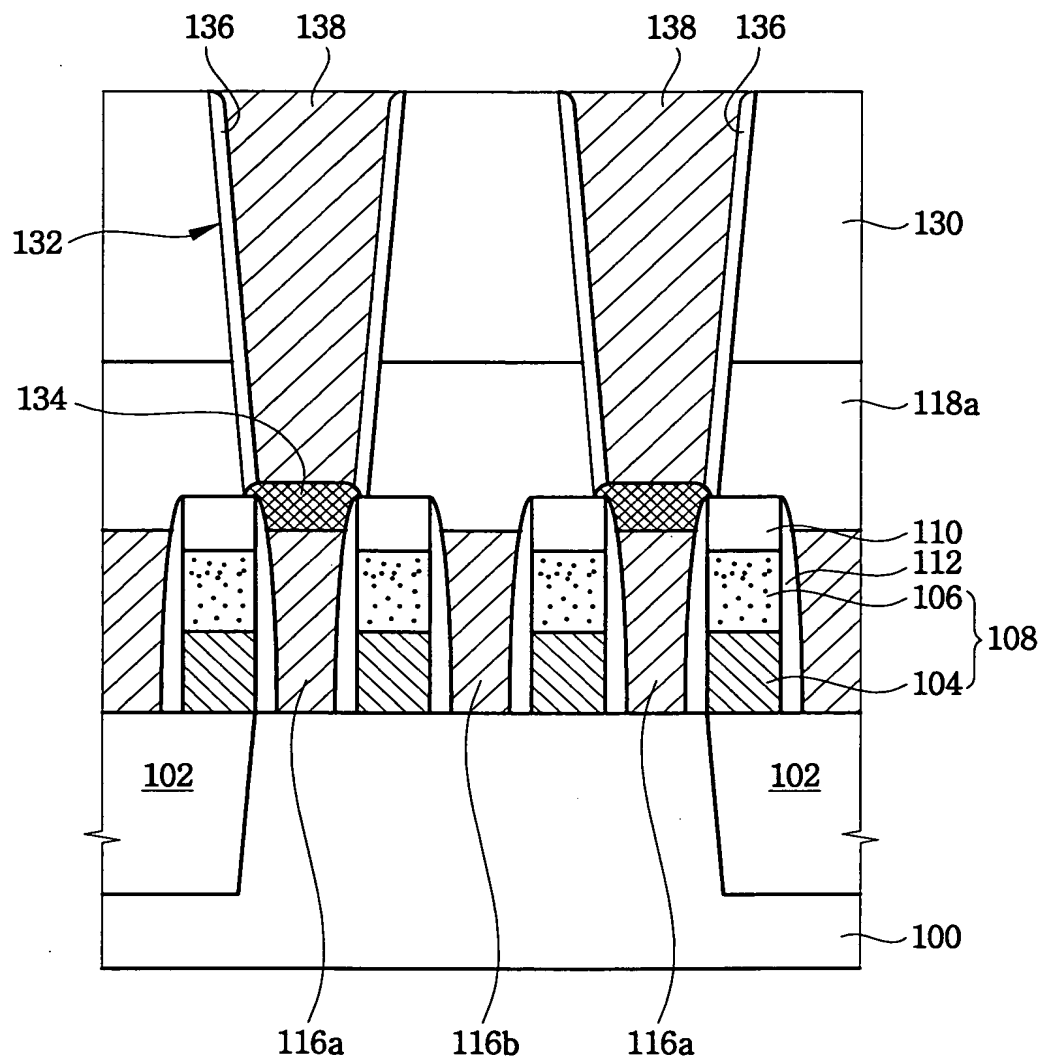
FIG. 10B





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FIG. 11A



This cross-sectional view shows a semiconductor device with a substrate 100. A gate stack 102 is formed on the substrate, featuring a tapered gate 114 and a gate cap 116a. The gate stack is surrounded by a dielectric layer 138. A conductive layer 134 is formed on top of the gate stack, and a conductive layer 124 is formed on top of the dielectric layer 138. A conductive layer 126 is formed on top of the conductive layer 124, and a conductive layer 136 is formed on top of the conductive layer 126. A conductive layer 128 is formed on top of the conductive layer 136. The device is shown in a cross-sectional view with a dashed line indicating a break in the substrate 100.